Refine Search

10/829,64

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Terms	Documents
L3 and (virgin adj polysilicon)	1

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US Pre-Grant Publication Full-Text Database
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Search History

DATE: Monday, August 30, 2004 Printable Copy Create Case

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DB=USPT; PLUR=YES; OP=ADJ			
L4	L3 and (virgin adj polysilicon)	1	L4
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L1	(high adj temperature) near2 (treatment or process)	21072	L1

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Search Results - Record(s) 1 through 1 of 1 returned.

1. Document ID: US 6727191 B2

L4: Entry 1 of 1 File: USPT Apr 27, 2004

US-PAT-NO: 6727191
DOCUMENT-IDENTIFIER: US 6727191 B2

TITLE: High temperature hydrogen anneal of silicon wafers supported on a silicon fixture

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw. D

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Terms	Documents
L3 and (virgin adj polysilicon)	1

Display Format: TI Change Format

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L4: Entry 1 of 1 File: USPT Apr 27, 2004

DOCUMENT-IDENTIFIER: US 6727191 B2
TITLE: High temperature hydrogen anneal of silicon wafers supported on a silicon fixture

Abstract Text (1):
A process for hydrogen annealing silicon wafers that have been cut from an ingot and polished on both sides, thereby removing crystal originated pits (COPs) in their surface. The wafers are then stacked in a tower having at least support surfaces made from virgin polysilicon, that is, polysilicon form by chemical vapor deposition, preferably from monosilane. The tower may include four virgin polysilicon legs have support teeth slotted along the legs and fixed at their opposed ends to bases. The wafers are supported at four equally distributed points at 0.707 of the wafer radius. The wafers so supported on the virgin polysilicon towers are annealed in a hydrogen ambient at 1250.degree. C. for 12 hours.

Brief Summary Text (15):
The invention includes an annealing method for removing defects from a stock silicon wafer after it has been cut from an ingot and preferably polished on both sides. A plurality of wafers are stacked in a support fixture, for example, a vertically extending tower, having at least support surfaces composed of silicon, preferably virgin polysilicon.

Brief Summary Text (16):
More preferably, the tower is composed of three or four silicon legs, preferably composed of virgin polysilicon, joined to two end bases. Slots are cut into the four legs to form inclined teeth having support surfaces disposed at locations corresponding to about 0.707 of the wafer radius. These locations equalize the mass of the wafer inside and outside of the support points. The support points for four legs are preferably arranged in a rectangular pattern centered, most preferably a square pattern, centered about the wafer center, thereby reducing wafer sag. The support points for three legs are preferably arranged in a pattern of an equilateral triangle centered on the wafer center.

Brief Summary Text (17):
The wafers supported in the silicon tower are subjected to a high-temperature anneal in a hydrogen ambient, for example, at 1250.degree. C. for 12 hours.

Brief Summary Text (18):
The tower may also be advantageously used for other processes involving high temperatures above 1100.degree. C. and may also be used for lower-temperature processes.

Detailed Description Text (3):
According to one aspect of the invention, a tower or boat used to support wafers in a high-temperature anneal of stock silicon wafers has at least support surfaces formed of silicon, preferably polysilicon, and more preferably virgin polysilicon. Boyle et al. have disclosed the fabrication of such a tower in U.S. patent application, Ser. No. 09/608,291, filed Jun. 30, 2000, now issued as U.S. Pat. No.

6,455,395, and incorporated herein by reference in its entirety. Virgin polysilicon is polycrystalline silicon formed by the chemical vapor deposition (CVD) of silane and/or chlorosilane. Virgin polysilicon is conventionally used as the source material for the Czochralski growth of monocrystalline silicon ingots. Although trichlorosilane (CHCl.sub.3) is the most prevalently used CVD precursor for semiconductor applications, virgin polysilicon formed from monosilane (SiH.sub.4) is preferred for towers because of the absence of trace amounts of chlorine. Virgin polysilicon of extraordinarily high purity is commercially available.

Detailed Description Text (4):
A form of a tower 10 is illustrated in the orthographic view of FIG. 1. It includes two bases 12, 14 and four legs 16, 18, 20, 22 permanently affixed at opposed ends to the two bases 12, 14. Preferably, at least the legs 16, 18, 20, 22 and, more preferably, also the bases 12, 14 are machined from separate pieces of silicon. The legs 16, 18, 20, 22 are more preferably machined from virgin polysilicon since they contact and support the wafers. The bases 12, 14 need not be fabricated from virgin polysilicon because they do not contact the silicon wafers. All the pieces are then joined together. The machining and joining processes are described in the cited patent application to Boyle et al. Each leg 16, 18, 20, 22 has a large number of generally parallel teeth 24, more clearly shown in the expanded orthographic view of FIG. 2 for the legs 18, 20 with short teeth 24b, which are machined into the legs to form slots 26 between the teeth 24. FIG. 1 has been simplified. In one product, 118 sets of teeth are spaced along about 1 m of a tower to support a large number of wafers 30 in a horizontal, parallel arrangement.

Detailed Description Text (7):
As shown in both the orthographic view of FIG. 1 and the axially sectioned view of FIG. 4, two legs 14, 16 having long teeth 24a projecting from their leg stems 32a are located on the side of the tower while two legs 18, 20 having shorter teeth 24b are located on the other side. The shorter teeth 24b project generally radially inwardly from their leg stems 32b with respect to the center of the tower 10 while the longer teeth 24a project towards the entry side of the tower to allow insertion of the wafers. The distance between the leg stems 32a of the longer-tooth legs 16, 22 is slightly larger than the diameter of the wafer 30 being inserted into the tower. This geometry allows all support surfaces 28a, 28b to form a square pattern at locations corresponding to about 0.707 (2.sup.-1/2) of the wafer radius. A rectangular pattern and more advantageously a square pattern reduce the maximum sag for points of the wafer far removed from the support surfaces. The radial position corresponds to a radius having an equal weight of wafer inside and out, thereby minimizing thermally induced sag and sag deformation and stress. A variation of 5% about this radius should introduce no significant problems, but in fact the support areas 28a, 28b are large enough to easily encompass the 0.707 position. Expansion slots 34 cut into the bases 14, 16 along the wafer insertion direction connected to a center relief circle 36 relieve any thermal stresses built up in the bases.

Detailed Description Text (9):
Such towers are capable of supporting wafers for extended periods in a high temperature anneal. The entire tower is formed of silicon so differential thermal expansion between it and the wafers is minimized. The silicon material, particularly at the supporting areas, has substantially the same hardness as the silicon wafers being supported. Accordingly, even if there is some dragging of the wafer on the tower surfaces, the dragging is unlikely to induce defects in the wafer. The placement of the teeth support surfaces minimizes sag and strain in the wafer, thereby reducing if not eliminating slip in the crystalline silicon wafer material. Because at least the legs may be formed of virgin polysilicon of very high purity, particularly in regards to heavy metals, impurity diffusion from the tower to the wafers is substantially eliminated.

Detailed Description Text (10):
Such a tower is consistent with the cited hydrogen anneal at 1250.degree. C. for 12

hours. Wafers are loaded into the above described silicon tower 10. The loaded tower 10 is placed in a conventional annealing oven 40, schematically illustrated in FIG. 5, which is controllably heated by resistive heaters 42 to the desired annealing temperature. Hydrogen and argon gas are flowed into the annealing oven 40 from gas supplies 44, 46 to supply the 25% H.sub.2 ambient that is substantially otherwise inert. The anneal is continued for the desired time of, for example, 12 hours.

CLAIMS:

1. A high-temperature annealing process, comprising the steps of: supporting a plurality of silicon substrates on a support fixture having support surfaces consisting essentially of silicon, wherein said support fixture comprises a plurality of legs composed of virgin polysilicon and including teeth projecting from stem portions of said legs, said support surfaces being formed at ends of said teeth; placing said support fixture supporting said silicon substrates into an annealing oven; flowing a hydrogen ambient into said annealing oven; and annealing said silicon substrates in said hydrogen ambient at an annealing temperature of at least 1100.degree. C.

2. The process of claim 1, wherein there are four of said legs and said support surfaces are disposed in a square pattern to support said substrates.

3. The process of claim 2, wherein said support surfaces are disposed in said square pattern at locations located at approximately 0.707 of four radii of said substrate.

9. A high-temperature wafer processing method, comprising the steps of: providing a tower comprising a plurality of legs comprising virgin polysilicon and each having a plurality of support areas cut therein along axial lengths thereof, and two bases fixed to opposed ends of said plurality of legs; supporting a plurality of silicon wafers on said support areas; and processing said supported silicon wafers at a processing temperature of at least 1100.degree. C.

11. The method of claim 10, wherein said plurality of legs consist of four legs and said support surfaces are disposed in a square pattern about a wafer center.

13. The method of claim 9, wherein said processing includes exposing said wafers to a hydrogen ambient at said processing temperature.

19. A high-temperature substrate treatment process, comprising the steps of: supporting a plurality of silicon substrates on a support fixture having support surfaces consisting essentially of silicon; placing said support fixture supporting said silicon substrates into an oven; and treating said silicon substrates in a hydrogen environment at a treatment temperature of at least 1100.degree. C. and continuing said treating for a predetermined extended length of time.

20. The process of claim 19, wherein said support surfaces are formed from members consisting essentially of virgin polysilicon.

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L4: Entry 1 of 1 File: USPT Apr 27, 2004

US-PAT-NO: 6727191
DOCUMENT-IDENTIFIER: US 6727191 B2

TITLE: High temperature hydrogen anneal of silicon wafers supported on a silicon fixture

DATE-ISSUED: April 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Zehavi; Raanan Y.	Sunnyvale	CA		
Boyle; James E.	Saratoga	CA		
Delaney; Laurence D.	Whitefish	MO		

US-CL-CURRENT: 438/795; 118/724, 257/E21.324

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Search History

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L5	L3 and radii	9	L5
L4	L3 and (virgin adj polysilicon)	1	L4
L3	L2 and ambient	74	L3
L2	L1 and (pattern near3 square)	132	L2
L1	(high adj temperature) near2 (treatment or process)	21072	L1

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☐ 1. Document ID: US 6773256 B2

L6: Entry 1 of 2 File: USPT Aug 10, 2004

US-PAT-NO: 6773256
DOCUMENT-IDENTIFIER: US 6773256 B2

TITLE: Ultra low NOx burner for process heating

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 2. Document ID: US 6727191 B2

L6: Entry 2 of 2 File: USPT Apr 27, 2004

US-PAT-NO: 6727191
DOCUMENT-IDENTIFIER: US 6727191 B2

TITLE: High temperature hydrogen anneal of silicon wafers supported on a silicon fixture

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L5 and angles	2

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L6: Entry 1 of 2 File: USPT Aug 10, 2004

DOCUMENT-IDENTIFIER: US 6773256 B2
TITLE: Ultra low NOx burner for process heating

Abstract Text (1):
An ultra low NOx burner for process heating is provided which includes a fluid based flame stabilizer which provides a fuel-lean flame at an equivalence ratio in the range of phi=0.05 to phi=0.3 and fuel staging lances surrounding the flame stabilizer in circular, flat, or load shaping profiles, each lance comprising a pipe having a staging nozzle at a firing end thereof, each lance having at least one hole for staging fuel injection, and each hole having a radial divergence angle and an axial divergence angle. The at least one hole and the divergence angles provide circular, flat or load shaping flame pattern. The burner provides NOx emissions of less than 9 ppmv at near stoichiometry combustion conditions.

Brief Summary Text (8):
In order to comply cost-effectively for NOx emissions, many combustion equipment manufacturers have developed LNBs. See, e.g., D. Keith Patrick, "Reduction and Control of NOx Emissions from High Temperature Industrial Processes", Industrial Heating, March 1998. The cost effectiveness of an LNB compared to the SCR system would generally depend on the type of burner, consistent NOx emissions from burner, burner costs and local compliance levels. In many ozone attainment areas, the LNBs (for >40 MM Btu/hr) have not been capable of producing low enough NOx emissions to comply with regulations or provide an alternative to SCR units. Therefore, SCR remains today as the only best available control technology for large process heaters and utility boilers.

Brief Summary Text (19):
In the present invention, an ultra low NOx burner for process heating is provided which includes a fluid based flame stabilizer which provides a fuel-lean flame at an equivalence ratio in the range of phi=0.05 to phi=0.3 and fuel staging lances surrounding the flame stabilizer with each lance having a pipe having a staging nozzle at a firing end thereof, each lance having at least one hole for staging fuel injection, and each hole having a radial divergence angle and an axial divergence angle. The burner generates NOx emissions of less than 9 ppmv at near stoichiometry conditions.

Brief Summary Text (20):
In one embodiment, the at least one hole and the divergence angles are adapted to provide complete circumferential coverage of the fuel-lean flame. In another embodiment, the at least one hole and the divergence angles are adapted to provide a flat flame pattern. In a third embodiment, the at least one hole and the divergence angles are adapted to provide a load shaping flame pattern

Brief Summary Text (21):
Preferably, between 4 and 16 staging lances are used and each staging nozzle has between 1 hole and 4 holes. Preferably the radial divergence angle is between 80 and 240 and the axial divergence angle is between 4.degree. and 16.degree.. The velocity of fuel exiting the nozzle is preferably between 300 to 900 feet per second for a natural gas staging fuel.

Doc. Entry 2 of 2 File: USPT Apr 27, 2004

DOCUMENT-IDENTIFIER: US 6727191 B2
TITLE: High temperature hydrogen anneal of silicon wafers supported on a silicon fixture

Abstract Text (1):
A process for hydrogen annealing silicon wafers that have been cut from an ingot and polished on both sides, thereby removing crystal originated pits (COPs) in their surface. The wafers are then stacked in a tower having at least support surfaces made from virgin polysilicon, that is, polysilicon form by chemical vapor deposition, preferably from monosilane. The tower may include four virgin polysilicon legs have support teeth slotted along the legs and fixed at their opposed ends to bases. The wafers are supported at four equally distributed points at 0.707 of the wafer radius. The wafers so supported on the virgin polysilicon towers are annealed in a hydrogen ambient at 1250.degree. C. for 12 hours.

Brief Summary Text (16):
More preferably, the tower is composed of three or four silicon legs, preferably composed of virgin polysilicon, joined to two end bases. Slots are cut into the four legs to form inclined teeth having support surfaces disposed at locations corresponding to about 0.707 of the wafer radius. These locations equalize the mass of the wafer inside and outside of the support points. The support points for four legs are preferably arranged in a rectangular pattern centered, most preferably a square pattern, centered about the wafer center, thereby reducing wafer sag. The support points for three legs are preferably arranged in a pattern of an equilateral triangle centered on the wafer center.

Brief Summary Text (17):
The wafers supported in the silicon tower are subjected to a high-temperature anneal in a hydrogen ambient, for example, at 1250.degree. C. for 12 hours.

Brief Summary Text (18):
The tower may also be advantageously used for other processes involving high temperatures above 1100.degree. C. and may also be used for lower-temperature processes.

Detailed Description Text (5):
As more clearly shown in the detailed elevational view of FIG. 3, the teeth 24a, 24b are cut to incline upwardly at a set angle of between 87.degree. and 891/2.degree. from the axis of the legs, but level support areas 28a, 28b are machined into the end of the teeth 24a, 24b to support a wafer 30 at a total of four points far removed from the leg stems 32a, 32b.

Detailed Description Text (7):
As shown in both the orthographic view of FIG. 1 and the axially sectioned view of FIG. 4, two legs 14, 16 having long teeth 24a projecting from their leg stems 32a are located on the side of the tower while two legs 18, 20 having shorter teeth 24b are located on the other side. The shorter teeth 24b project generally radially inwardly from their leg stems 32b with respect to the center of the tower 10 while

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1. Document ID: US 6773256 B2

L5: Entry 1 of 9 File: USPT Aug 10, 2004

US-PAT-NO: 6773256
DOCUMENT-IDENTIFIER: US 6773256 B2

TITLE: Ultra low NOx burner for process heating

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

2. Document ID: US 6762543 B1

L5: Entry 2 of 9 File: USPT Jul 13, 2004

US-PAT-NO: 6762543
DOCUMENT-IDENTIFIER: US 6762543 B1

TITLE: Diamond diode devices with a diamond microtip emitter

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

3. Document ID: US 6727191 B2

L5: Entry 3 of 9 File: USPT Apr 27, 2004

US-PAT-NO: 6727191
DOCUMENT-IDENTIFIER: US 6727191 B2

TITLE: High temperature hydrogen anneal of silicon wafers supported on a silicon fixture

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

4. Document ID: US 6500760 B1

L5: Entry 4 of 9 File: USPT Dec 31, 2002

US-PAT-NO: 6500760
DOCUMENT-IDENTIFIER: US 6500760 B1

TITLE: Gold-based electrical interconnections for microelectronic devices

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6132278 A

L5: Entry 5 of 9 File: USPT Oct 17, 2000

US-PAT-NO: 6132278
DOCUMENT-IDENTIFIER: US 6132278 A

TITLE: Mold method for forming vacuum field emitters and method for forming diamond emitters

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 6. Document ID: US 5840402 A

L5: Entry 6 of 9 File: USPT Nov 24, 1998

US-PAT-NO: 5840402
DOCUMENT-IDENTIFIER: US 5840402 A

TITLE: Metallized laminate material having ordered distribution of conductive through holes

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 7. Document ID: US 5675471 A

L5: Entry 7 of 9 File: USPT Oct 7, 1997

US-PAT-NO: 5675471
DOCUMENT-IDENTIFIER: US 5675471 A

TITLE: Characterization, modeling, and design of an electrostatic chuck with improved wafer temperature uniformity

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 8. Document ID: US 4886118 A

L5: Entry 8 of 9 File: USPT Dec 12, 1989

US-PAT-NO: 4886118
DOCUMENT-IDENTIFIER: US 4886118 A

TITLE: Conductively heating a subterranean oil shale to create permeability and subsequently produce oil

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 9. Document ID: US 4840810 A

L5: Entry 9 of 9 File: USPT Jun 20, 1989

US-PAT-NO: 4840810
DOCUMENT-IDENTIFIER: US 4840810 A

TITLE: Process for the preparation of an edible fat-containing product

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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Terms	Documents
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